A CMOS Power Amplifier for 5G Application

Seungwon Park and Sanggeun Jeon
School of Electrical Engineering, Korea University, Seoul 136-713, Korea

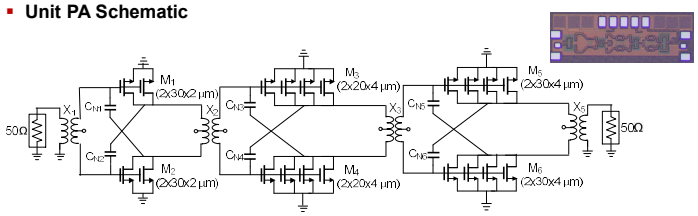
Introduction

- Power amplifier (PA) is one of the most challenging RF blocks in CMOS technology
  - Due to low breakdown voltage and high substrate loss
- Several CMOS mm-wave PAs have been reported as the gate length scales down [1]-[2]

[1] M. Motoyoshi and M. Fujishima, "46 GHz differential power amplifier with 11 GHz bandwidth using on-chip transformer," *in Proc. IEEE Int. Symp. Radio-Freq. Integr. Technol.*, Aug. 2014, pp. 1 – 3.
[2] J. Lin, C. C. Boon, X. Yi and G. Feng, "A 50-59 GHz CMOS injection locking power amplifier," *IEEE Microw. Wireless Comp. Lett.*, vol. 25, no. 1, pp. 52 – 54, Jan. 2015.

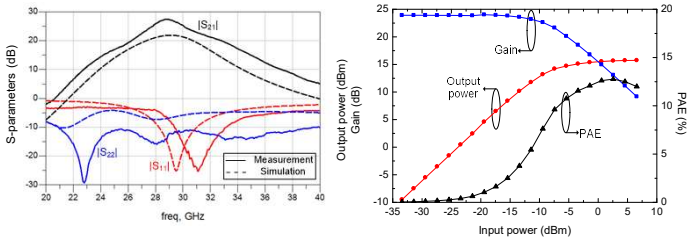
Design

- Unit PA Schematic



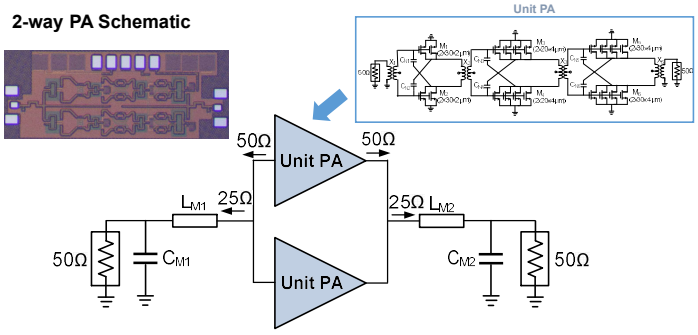
  - 3-stage differential power amplifier
  - Each transistor cell is composed of two or four unit transistors combined for high operating frequency and output power
  - The input, inter-stage and output matching network are all implemented by transformer for low loss and compact size

- Unit PA Measurement



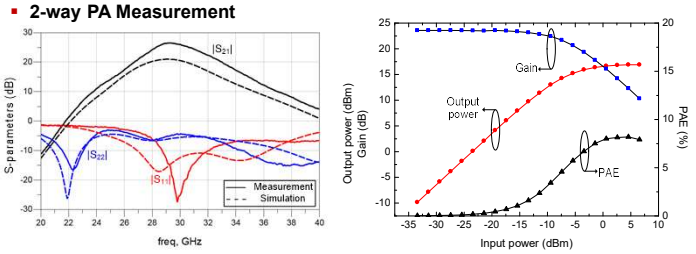
- The measurement exhibits a peak gain of 27.4 dB
- The 3-dB bandwidth is 2.4 GHz from 27.6 GHz to 30.2 GHz
- The saturation output power and peak PAE are measured at 15.7 dBm and 12.8 %, respectively, at 30 GHz.

- 2-way PA Schematic



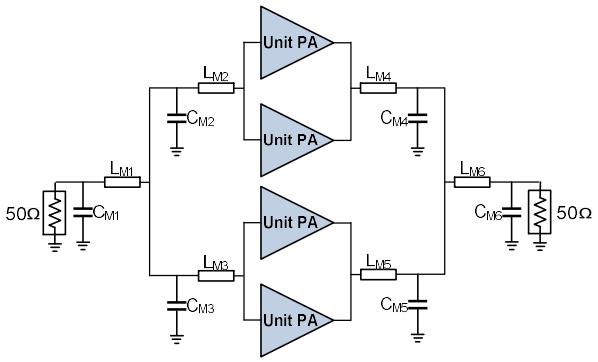
- Because of current combining structure, the transistor-load impedance seen looking into transistor drain to load is changed by output current of auxiliary and main amplifiers.
- To overcome above problem, L-section matching network is used to make load impedance 25 Ohm

- 2-way PA Measurement

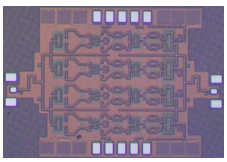


- The measurement exhibits a peak gain of 26.5 dB
- The saturation output power and peak PAE are measured at 17 dBm and 8.2 %, respectively, at 30 GHz.

- 4-way PA Schematic

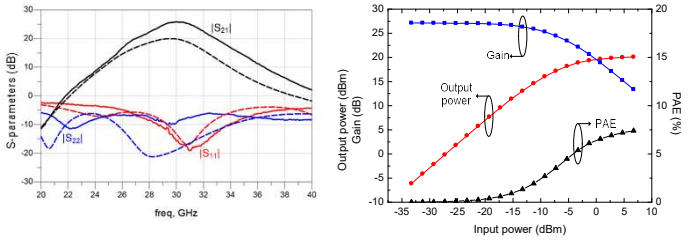


Results



- Samsung 65-nm CMOS

- The measurement exhibits a peak gain of 25.7 dB
- The 3-dB bandwidth is 3.7 GHz from 28.2 GHz to 31.9 GHz
- The saturation output power and peak PAE are measured at 20.1 dBm and 7.3 %, respectively, at 30 GHz.



Conclusion

- A CMOS PA is fabricated in a 65-nm CMOS technology
- The peak output power and PAE are measured 20.1 dBm and 7.3 %, respectively

The authors thank IDEC for MPW and CAD tool support